IN THE CLAIMS:

Please amend claims 3 and 8 in accordance with the Certificate of Correction issued in Patent No. 5,961,614, and add new claims 11 through 26:

3. (Amended) A method as claimed in claim [[1]] 2 wherein said memory access controller waits until said bit reflects a value of said data status signal indicating successful transmission of a data unit to the external system before sending another data unit.

8. (Amended) A computer system comprising:

a computer system memory;

an I/O device connected to an external system to transfer data units between said computer system memory and an external system[[;]], said I/O device including a data status signal generator which generates a data status signal upon completion of transfer of a data unit;

a memory access controller connected to said computer system memory and said I/O device; said memory access controller including a register for storing status information which the memory access controller uses to control its own operation, wherein said memory access controller receives said data status signal and stores an indication of a value of said data status signal in said register, wherein during a data transmit operation the memory access controller retrieves said data unit from said computer system memory and transfers said data unit to said I/O device and said I/O device transmits said data unit to said external system and wherein the said data transfer status signal is sent from the I/O device to the memory access controller after the transfer of said data unit to said I/O device.

11. (New) The method of claim 1 wherein the data status signal indicates the end of the data unit.

12. (New) The method of claim 1 wherein the data status signal is used to control the operation of the memory access controller.

13. (New) The method of claim 1 wherein the memory access controller executes an instruction in response to the data status signal.

14. (New) The method of claim 1 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

15. (New) The method of claim 1 wherein the data status signal is used to keep a channel process active.

16. (New) The system of claim 8 wherein the data status signal indicates the end of the data unit.

17. (New) The system of claim 8 wherein the data status signal is used to control the operation of the memory access controller.

18. (New) The system of claim 8 wherein the memory access controller executes an instruction in response to receipt of the data status signal.

19. (New) The system of claim 8 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

20. (New) The system of claim 8 wherein the data status signal is used to keep a channel process active.

21. (New) A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:

a register for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to an external system; and

circuitry coupled to the register for receiving the data status signal and for controlling subsequent operation of the memory access controller based on the data status signal.

22. (New) The controller of claim 21 wherein the data status signal indicates the end of the data unit.

23. (New) The controller of claim 21 wherein the memory access controller executes an instruction in response to the data status signal.

24. (New) The controller of claim 21 wherein the data status signal is used to prompt the memory access controller to request information from the I/O device.

25. (New) The controller of claim 21 wherein the data status signal is used to keep a channel process active.

26. (New) A memory access controller adapted to be coupled to a computer system memory and an Input/Output (I/O) device, comprising:

means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to an external system; and

means for controlling subsequent operation of the memory access controller using the data status signal.

STATUS OF CLAIMS AND SUPPORT FOR CLAIM CHANGES

Original claims 1-10 are in the patent as corrected by the Certificate of Correction and new claims 11-26 are pending.

Applicants have added new claims 11-26, which are directed to a memory access controller. Support for new claims 11-26 can be found in the specification of the issued patent at column 3, line 57 through col. 6, line 17 et seq. and in Figures 1-8.

Respectfully submitted,
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